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<input type="checkbox"/>	L9	vliw or long instruction or large instruction	3718
<input type="checkbox"/>	L8	sampl\$3 and L7	27
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**1. Fine grain mapping strategy for multiprocessor systems**Shieh, J.J.; Papachristou, C.A.;
Computers and Digital Techniques, IEE Proceedings-
Volume 138, Issue 3, May 1991 Page(s):109 - 120[AbstractPlus](#) | Full Text: [PDF](#)(840 KB) IEEE JNL**2. A portable PXI platform for mobile applications [military test systems]**Chuang, C.;
AUTOTESTCON 2003. IEEE Systems Readiness Technology Conference. Pro
22-25 Sept. 2003 Page(s):104 - 107
Digital Object Identifier 10.1109/AUTEST.2003.1243562[AbstractPlus](#) | Full Text: [PDF](#)(446 KB) IEEE CNF[Help](#) [Contact Us](#) [Privacy & :](#)

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IEEE STD IEEE Standard

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- ☐ 1. **Functional units with conditional input/output behavior in VLIW processors**
 Bekooij, M.J.G.; Engels, L.J.M.; van der Werf, A.; Busa, G.;
 Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001
 13-16 March 2001 Page(s):822
 Digital Object Identifier 10.1109/DATE.2001.915171
[AbstractPlus](#) | Full Text: [PDF\(64 KB\)](#) IEEE CNF
- ☐ 2. **Run-time energy estimation in system-on-a-chip designs**
 Haid, J.; Kaefer, G.; Steger, Ch.; Weiss, R.;
 Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asi
 Pacific
 21-24 Jan. 2003 Page(s):595 - 599
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IEEE CNF IEEE Conference Proceeding

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- ☐ 1. **An instruction cache architecture for parallel execution of Java threads**
 Wanming Chu; Yamin Li;
 Parallel and Distributed Computing, Applications and Technologies, 2003. PDC
 Proceedings of the Fourth International Conference on
 27-29 Aug. 2003 Page(s):180 - 184
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**1. Power4 system design for high reliability**Bossen, D.C.; Tendler, J.M.; Reick, K.;
Micro, IEEE

Volume 22, Issue 2, March-April 2002 Page(s):16 - 24

Digital Object Identifier 10.1109/MM.2002.997876

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(269 KB\)](#) IEEE JNL**2. IBM Power5 chip: a dual-core multithreaded processor**Kalla, R.; Balaram Sinharoy; Tendler, J.M.;
Micro, IEEE

Volume 24, Issue 2, Mar-Apr 2004 Page(s):40 - 47

Digital Object Identifier 10.1109/MM.2004.1289290

[AbstractPlus](#) | Full Text: [PDF\(404 KB\)](#) IEEE JNL**3. Stretching the limits of clock-gating efficiency in server-class processors**Jacobson, H.; Bose, P.; Zhigang Hu; Buyuktosunoglu, A.; Zyuban, V.; Eickeme
Griswell, J.; Logan, D.; Balaram Sinharoy; Tendler, J.;High-Performance Computer Architecture, 2005. HPCA-11. 11th International :
12-16 Feb. 2005 Page(s):238 - 242

Digital Object Identifier 10.1109/HPCA.2005.33

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1 [Poster session: Bottleneck analysis in java applications using hardware performance](#)

[monitors](#)

Dries Buytaert, Andy Georges, Lieven Eeckhout, Koen De Bosschere

 October 2004 **Companion to the 19th annual ACM SIGPLAN conference on Object-oriented programming systems, languages, and applications**

Publisher: ACM Press

 Full text available: [pdf\(128.74 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This poster presents `MonitorMethod` which helps Java programmers gain insight in the behavior of their applications. `MonitorMethod` instruments the Java application and relates hardware performance monitors (HPMs) to the methods in the Java application's source code. We present a detailed case study showing that linking microprocessor-level performance characteristics to the source code is helpful for identifying performance bottlenecks and their causes. In add ...

Keywords: java, performance analysis, phase behavior, profiling

2 [Vertical profiling: understanding the behavior of object-oriented applications](#)



Matthias Hauswirth, Peter F. Sweeney, Amer Diwan, Michael Hind

 October 2004 **ACM SIGPLAN Notices , Proceedings of the 19th annual ACM SIGPLAN conference on Object-oriented programming, systems, languages, and applications OOPSLA '04**, Volume 39 Issue 10

Publisher: ACM Press

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Object-oriented programming languages provide a rich set of features that provide significant software engineering benefits. The increased productivity provided by these features comes at a justifiable cost in a more sophisticated runtime system whose responsibility is to implement these features efficiently. However, the virtualization introduced by this sophistication provides a significant challenge to understanding complete system performance, not found in traditionally compiled languages ...

Keywords: hardware performance monitors, perturbation, software performance monitors, vertical profiling, whole-system analysis